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Thread-like CMOS logic circuits using SWCNT transistors for e-textile systems

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Recently, wearable electronic textile (e-textile) devices have been spotlighted for next generation smart devices and systems because of their unique advantages such as light, deformability in movement, and wide range application with various fields. Fibre-based electronics, formed directly on textile substrates, is the one of most desirable features required for wearable e-textile since we can integrate sensing and processing circuitry onto the garments.

Typical fibre-based electronics can be formed on a premade two-dimensional (2-D) fabrics. The most advantage of this approach is that device fabrication process is similar and compatible with conventional silicon-based process technology. However, due to the rough surface morphology and weakly interfacial adhesion between the deposited film and fabric, 2-D fabric electronics are limited in terms of device performance and integration with a large scale electronics. Another approach is forming transistors on a thread-like cylindrical single fibre. Since the transistors are formed on the thread, there is no performance degradation due to the rough surface. Furthermore, the fabrication process of the thread-like fibre electronics is compatible with the existing textile fabrication process - a simple reel-to-reel process and weaving technology. Thus, we can easily integrate e-textile with conventional garments.

However, integration of logic-gates and large-scale circuits using the thread-like electronics is still challenging. This limitation greatly prohibits the use of the thread-like electronics in practical applications. We previously demonstrated thread-like single-walled carbon nanotube (SWCNT) fibre-type thin-film transistors (TFTs) as well as CMOS logic circuits using the SWCNT TFTs using partial reel coating and selective doping process. In this talk, we will introduce the fabrication process of SWCNT TFTs and dynamic operation of the CMOS logic circuits based on SWCNT TFTs. We will also discuss SPICE simulations techniques about how to optimize threshold voltage, contact resistance, off-/gate leakage current of the TFTs.

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